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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,310	06/23/2003	Masaki Hashimura	T36-156800M/RS	7969

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EXAMINER	
LE, DUNG ANH	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,310	HASHIMURA ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *6-11 and 19-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *2,3,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-6 and 12- 18 are pending. This is a new ground of rejection bases new applied references.

Claim Rejections

Set of claims 1-6.

Claims 1 and 5 are rejected under 35 USC 102 (b) as being anticipated by Sasaki et al. (5,888,883).

Regarding claim 1, Sasa ki et al. (5,888,883) teaches a method of producing a plurality of semiconductor elements by individually dividing said semiconductor elements formed on a substrate, said method comprising:

removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near said substrate remains or (ii) no semiconductor layers remains on said parting lines;

forming a protective film (col 1, lines 25-30)so that said semiconductor layers are covered with said protective film and said protective film can be removed by an after-process;

scanning said substrate with a laser beam (col 1, lines 30- 40) along said parting lines to form separation grooves in a front surface of said substrate; and removing said protective film and unnecessary products produced by said laser beam scanning,

wherein said separation grooves formed along said parting lines by said laser beam scanning are used for dividing said substrate into individual semiconductor elements (col 45-50).

Regarding claim 5, wherein a rear surface of said substrate is polished to reduce the thickness of said substrate after the protective film and unnecessary product removal so that said substrate can be divided into individual semiconductor elements by use of only said separation grooves formed in said front surface of said substrate (fig 10 and related texts).

Claims 1, 4 are rejected under 35 USC 102 (e) as being anticipated by Fujii et al. (6805808).

Regarding claims 1, Fugii et al. teaches a method of producing a plurality of semiconductor elements by individually dividing said semiconductor elements formed on a substrate, said method comprising:

removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near said substrate remains or (ii) no semiconductor layers remains on said parting lines;

forming a protective film 5/8 (Figs. 2(a)-(f), col 1 and related texts)) so that said semiconductor layers are covered with said protective film and said protective film can be removed by an after-process (col 5, lines 5-10);

scanning said substrate with a laser beam (col 1, lines 30- 40) along said parting lines to form separation grooves 6 in a front surface of said substrate; and removing said protective film and unnecessary products produced by said laser beam scanning,

wherein said separation grooves formed along said parting lines by said laser beam scanning are used for dividing said substrate into individual semiconductor elements (fig.2f and related texts).

Regarding claim 4, wherein rear grooves corresponding to said separation grooves 9 are formed in a rear surface of said substrate after the protective film 5/8 and unnecessary product removal (fig. 2f and related texts).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Fujii et al. (6805808) in view of the following remark.

Regarding claim 6, Fujii et al. teaches the claimed invention as applied to claim 1 including wherein a rear surface of said substrate is polished said substrate after the

protective film and unnecessary product removal and rear grooves corresponding to said parting lines are then formed in a rear surface of said substrate (Figs. 2c- 2f and related texts)) except for a rear surface of said substrate is polished to reduce the thickness of said substrate as cited in current claim.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to polish a rear surface of said substrate to reduce the thickness of said substrate Fugii 's method in order to obtain the best trenches in rear surface of the substrate to simplify the breaking operation of the wafer to be performed in the latter part of the process.

Regarding claims 2-3, see Reasons for Indication of Allowable Subject Matter below.

Set of claims 12- 18

Claims 12 and 17 are rejected under 35 USC 102 (b) as being anticipated by Sasaki et al. (5,888,883).

Regarding claim 12, Sasa ki et al. teaches a method of producing a plurality of semiconductor elements by individually dividing said semiconductor elements formed on a substrate, said method comprising:

removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near to said substrate remains on said parting lines or (ii) there is no semiconductor layer on said parting lines; and

scanning said substrate along said parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves (col 1, lines 30-35),

wherein said broken line-shaped or dot line-shaped separation grooves formed by laser beam scanning along the parting lines are used so that said substrate is divided into individual semiconductor elements (col 1, lines 45-50).

Regarding claim 17, wherein before said separation grooves are used for dividing said substrate into elements, a rear surface of said substrate is polished to reduce a thickness of said substrate so that said substrate can be divided into individual semiconductor elements only by said separation grooves formed in the front surface of said substrate (fig. 10 and related texts).

Claims 12 and 15, 16 are rejected under 35 USC 102 (e) as being anticipated by Fujii et al. (6805808).

A Fujii et al. teaches a method of producing a plurality of semiconductor elements by individually dividing said semiconductor elements formed on a substrate, said method comprising:

removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near to said substrate remains on said parting lines or (ii) there is no semiconductor layer on said parting lines; and

scanning said substrate along said parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves 6 (figs. 2a- 2f and related texts) , wherein said broken line-shaped or dot line-shaped separation grooves formed by laser beam scanning along the parting lines are used so that said substrate is divided into individual semiconductor elements (fig.2f and related texts) .

Regarding claim 15, forming a protective film 5/8 (fig. 2c and related texts) so that layers formed on a front surface side of said substrate are covered with said protective film before the laser beam scanning and said protective film can be removed by an after-process; and removing said protective film and unnecessary products produced due to laser beam scanning after the laser beam scanning (fig. 2e and col 5, lines 5-10).

Regarding claim 16, wherein before said separation grooves are used for dividing said substrate into elements, rear grooves 9 corresponding to said parting lines are formed in a rear surface of said substrate (fig. 2f and related texts) .

Claim 18 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Fujii et al. (6805808) in view of the following remark.

Fujii et al. teaches the claimed invention as applied to claim 1 including wherein a rear surface of said substrate is polished said substrate after the protective film and unnecessary product removal and rear grooves corresponding to said parting lines are then formed in a rear surface of said substrate (Figs. 2c- 2f and related texts)) except for a rear surface of said substrate is polished to reduce the thickness of said substrate as cited in current claim.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to polish a rear surface of said substrate to reduce the thickness of said substrate Fugii 's method in order to obtain the best trenches in rear surface of the substrate to simplify the breaking operation of the wafer to be performed in the latter part of the process.

Regarding claims 13-14, see Reasons for Indication of Allowable Subject Matter below.

Reasons for Indication of Allowable Subject Matter

Claims 2- 3 and 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record

and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Sasaki et al. (U.S. Patent No. 5,888,883) and Fujii et al. (U.S. Patent No. 6,805,808) and Background of Invention , taken individually or in combination, do not teach the claimed invention having the semiconductor layer removal is carried out in an electrode-forming etching process for exposing an electrode-forming portion of an electrode-forming layer on a side near said substrate by etching and wherein in the semiconductor layer removal, electrode-forming layer side part of said substrate on said parting lines is also removed by dicing.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, M. Smith can be reached on (571) 272-1907. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818